AMENDMENTS TO THE CLAIMS

1. (original) An apparatus comprising:

a first pinned photodiode formed in a semiconductor substrate;

a first transfer transistor placed between the first pinned photodiode and an output node, the combination of said first pinned photodiode and first transfer transistor forming a first light sensing pixel;

a second pinned photodiode formed in said semiconductor substrate;

a second transfer transistor placed between the second pinned photodiode and said output node, the combination of said second pinned photodiode and second transfer transistor forming a second light sensing pixel;

a reset transistor coupled between a voltage reference and the output node; and

an output transistor that is coupled to the output node.

2. (original) The apparatus of Claim 1 wherein the voltage reference is selectable between a low voltage reference V_{ss} or high voltage reference V_{ref}.

3. (original) The apparatus of Claim 1 wherein said first light sensing pixel is in a first row of an imaging array and said second light sensing pixel is in a second row of an image array adjacent to said first row.

4. (original) The apparatus of Claim 1, wherein the output transistor is connected to a column line out without the use of a row select transistor.

5. (original) The apparatus of Claim 1, further including:

a third pinned photodiode formed in said semiconductor substrate;

a third transfer transistor placed between the third pinned photodiode and said output node, the combination of said third pinned photodiode and third transfer transistor forming a third light sensing pixel;

6. (original) The apparatus of Claim 1, wherein said reset transistor is operative to reset said output node to a low voltage prior to transferring a signal from either said first or second photodiode.

7. (original) The apparatus of Claim 1, wherein said output transistor has its gate coupled to said output node.

8. (original) A CMOS sensing array comprising:

a plurality of pixels arranged in rows and columns formed in a semiconductor substrate each comprising:

(a) a pinned photodiode;

(b) a transfer transistor for transferring a signal out from the pinned photodiode;

a plurality of output nodes, each of said output nodes shared between at least two of said pixels and for receiving said signal from said at least two of said pixels;

a plurality of reset transistors associated with said plurality of output nodes, each of said reset transistors shared between said at least two of said pixels and coupled between a voltage reference and an associated output node; and

a plurality of output transistors associated with said plurality of output nodes , each of said output transistors shared between said at least two of said pixels, the gate of the output transistor being coupled to the associated output node.

9. (original) The apparatus of Claim 8 wherein the voltage reference is selectable between a low voltage reference V_{ss} or high voltage reference V_{ref}.

10. (original) The imaging array of Claim 8 further including a processing circuit for receiving the output of said output transistors.

11. (original) The imaging array of Claim 10 further including an I/O circuit for outputting the output of said output transistors pixels off of said CMOS image sensor.

12. (original) The imaging array of Claim 9 wherein said output nodes share pixels that are from adjacent rows from the same column.

13. (original) The imaging array of Claim 9 wherein the output transistors are connected to a column line out without the use of a row select transistor.